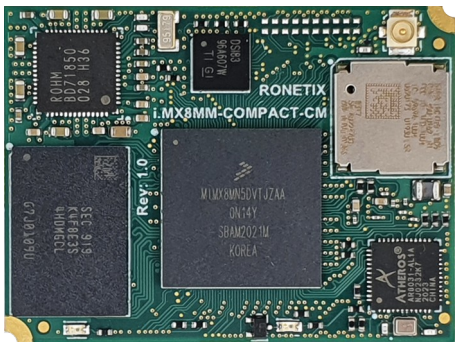
RONETIX
DEVELOPMENT TOOLS

i.MX8MM-COMPACT-CM

CPU Module (SoM) with NXP i.MX8M-MINI

Datasheet

rev 1.0



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1. Document Revision History

Revision	Date	Notes
1.0	20-Jun-2021	Initial release

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3. Overview

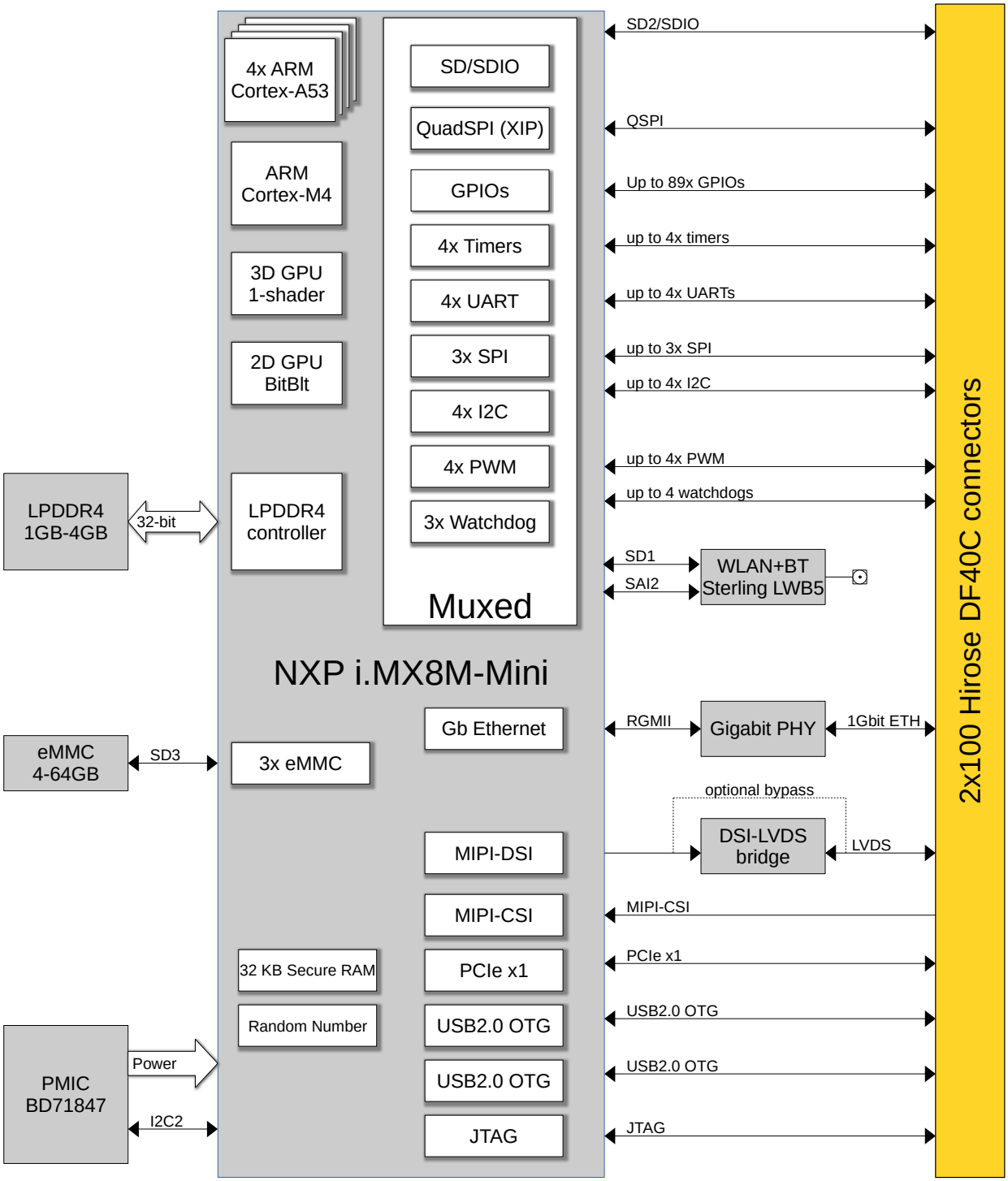
3.1 General Information

The **i.MX8MM-COMPACT-CM** is a high-performance processing for low-power CPU Module (SoM – System On Module) that perfectly fits various embedded products of connected and portable devices. It is based on the NXP i.MX8M-Mini family of multipurpose processors from which feature a quad ARM® Cortex™-A53 up to 2GHz + an additional ARM Cortex-M4. This Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux on the Cortex-A53 core and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

3.2 Highlights

CPU	• Quad Armv8-A, 64-bit Cortex™-A53 Core, 2GHz • ARM® Cortex™-M4, 400MHz
Memory	• RAM: 1 GiB LPDDR4 (optional: up to 4 GiB) • eMMC: 4 GiB (optional: up to 64 GiB)
Display	• LVDS, up to 1400 x 1050 @60Hz • MIPI DSI
Camera	• MIPI-CSI, 4 data lanes
Network	• Ethernet: 10/100/1000Mbps • WiFi: Sterling LWB5, 802.11ac, dual band (optional) • Bluetooth: Bluetooth 4.2 (optional)
I/O	• PCIe 2.0, 1-lane • 2x USB2.0 OTG port • Up to 4x UART ports • MMC/SD/SDIO • Up to 3x SPI • Up to 4x I2C • Up to 4x general purpose PWM signals • GPIOs
Electrical	• Supply Voltage: 3.85 – 5.0V
Physical	• Board size: 40x30mm • Operation temperature: 0° +70°C, -20° to 85° C (optional) • Relative humidity: 10% to 90%

3.3 SoM Block Diagram



4. CPU Module Hardware Components

This chapter describes the hardware components of i.MX8MM-COMPACT-CM SoM.

4.1 Power supply

i.MX8MM-COMPACT-CM uses Rohm's BD71847 as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8M series of application processors. The PMIC regulates all power rails required on CPU module from a single 3.85V-5.0V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

4.2 CPU i.MX8M-MINI

The i.MX 8M-MINI Dual / 8M Quad processors represent NXP's latest market of connected streaming audio/video devices, scanning/imaging devices, and various devices requiring high-performance, low-power processors. The i.MX 8M-MINI Dual / 8M Quad processors feature advanced implementation of a quad Arm®Cortex®-A53 core, which operates at speeds of up to 2 GHz. A general purpose Cortex®-M4 core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3Lmemory. There are a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

4.2.1 CPU Block Diagram

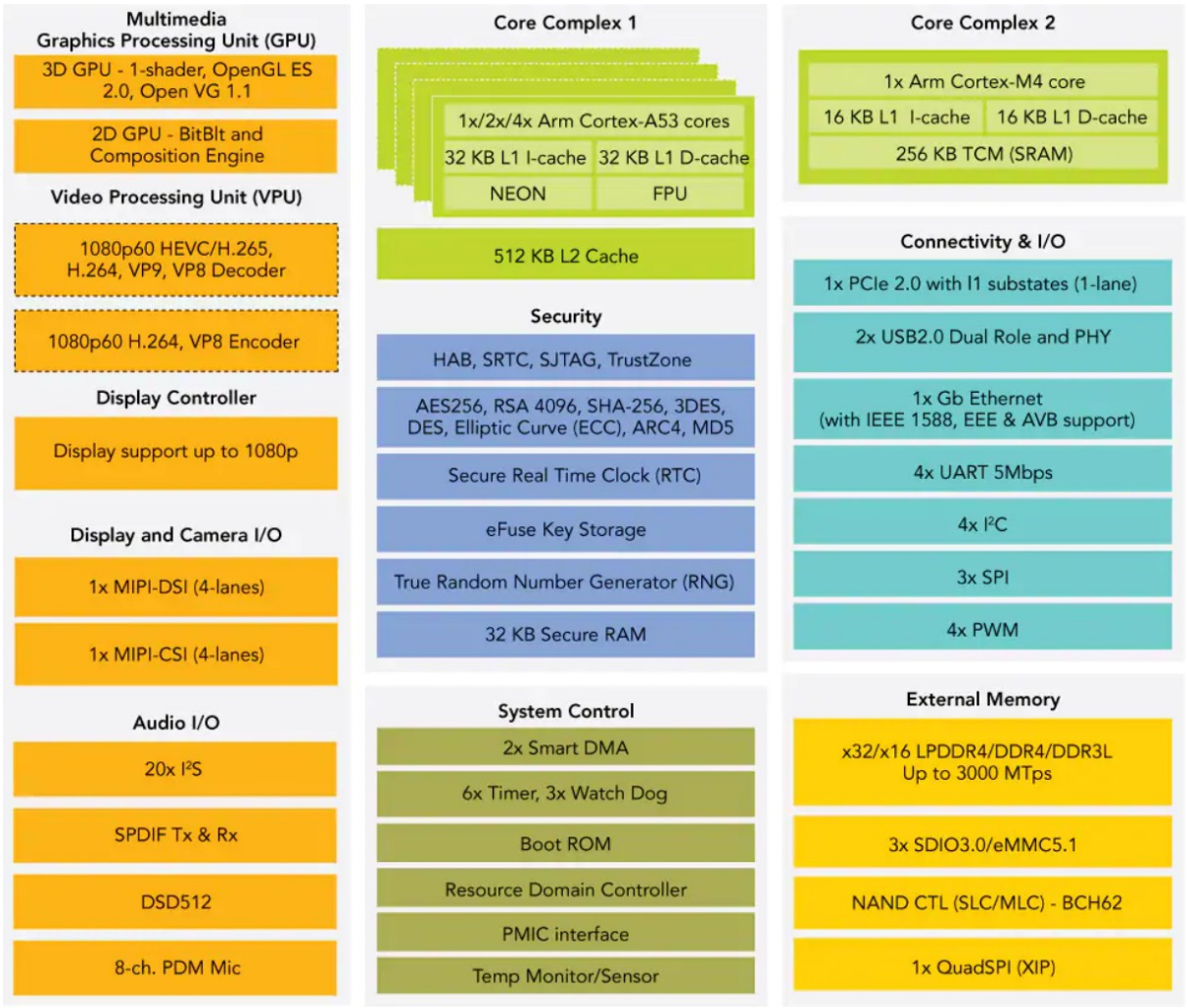


Figure 4.1: i.MX8M-MINI block diagram

4.2.2 CPU Platform

The i.MX8M-MINI processor implements up to four ARM® Cortex®-A53 cores intended for high level O/S, with an ARM® Cortex®-M4 core dedicated for real-time tasks.

The ARM Cortex-A53 MPCore™ platform has the following features:

- Quad ARM Cortex-A53 Cores
- Target frequency of 2GHz
- The core configuration is symmetric, where each core includes:

  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - MPE (media processing engine) with NEON co-processor supporting SIMD architecture
- The Arm Cortex-A53 Core complex shares:
  - General interrupt controller (GIC) with 128 interrupt support
  - Global timer
  - Snoop control unit (SCU)
  - 1 MB unified I/D L2 cache
  - NEON MPE co-processor
    - SIMD Media Processing Architecture
    - NEON register file with 32x64-bit general-purpose registers
    - NEON Integer execute pipeline (ALU, Shift, MAC)
    - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
    - NEON load/store and permute pipeline

The ARM Cortex-M4 platform includes the following features:

- Cortex-M4 CPU core operating at 400 MHz
- MPU (memory protection unit)
- FPU (floating-point unit)
- 16 KByte instruction cache
- 16 KByte data cache
- 256 KByte TCM (tightly-coupled memory)

4.3 Memory

4.3.1 DRAM

i.MX8MM-COMPACT-CM is standard equipped with 1 GB LPDDR4 memory. Optionally up to 4 GB can be assembled. The data bus is 32-bit wide.

4.3.2 eMMC – non-volatile storage memory

i.MX8MM-COMPACT-CM is standard equipped with 4 GB eMMC. Optionally up to 32 GB can be assembled.

The eMMC can be used as boot device.

4.4 Gigabit Ethernet

i.MX8MM-COMPACT-CM implements one full-featured 10/100/1000 Ethernet ports implemented with MAC built into the i.MX8M-MINI SoC, coupled with AR8031 RGMII Ethernet PHYs from Qualcomm. The Ethernet interface support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

4.5 WLAN

i.MX8MM-COMPACT-CM optional wireless communication is implemented with Laird Sterling LWB5 WLAN module. Sterling-LWB5 is an 802.11ac/b/g/n Dual-Band Wi-Fi+Bluetooth module based on Cypress's BCM43353 chipset. It is Dual-Band AC on 2.4GHz + 5GHz and incorporates Bluetooth 4.2. The download speed are 300Mbps on N networks and 867Mbps on AC network.

i.MX8MM-COMPACT-CM is equipped with a U.FL high frequency connector for external antenna.

4.6 LVDS bridge

i.MX8MM-COMPACT-CM implements (optional) onboard LVDS display interface by converting the MIPI-DSI to LVDS signals using Texas Instruments SN65DSI83 transceiver. The SN65DSI83 DSI to FlatLink bridge device features a single-channel MIPI D-PHY receiver front-end configuration with four lanes per channel operating at 1 Gbps per lane; a maximum input bandwidth of 4 Gbps. The bridge decodes MIPI DSI18 bpp RGB666 and 24 bpp RGB888 packets and converts the formatted video data stream to a FlatLink compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Single-Link LVDS with

four data lanes per link. The SN65DSI83 device can support up to WUXGA1920 × 1200 at 60 frames per second, at 24 bpp with reduced blanking. The SN65DSI83 device is also suitable for applications using 60 fps 1366 × 768 /1280 × 800 at 18 bpp and 24 bpp. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces. Designed with industry-compliant interface technology, the SN65DSI83 device is compatible with a wide range of microprocessors, and is designed with a range of power management features including low-swing LVDS outputs, and the MIPI defined ultra-low power state (ULPS) support.

Main features:

- LVDS Output Clock Range of 25 MHz to 154MHz.
- Suitable for up to 60 fps WUXGA 1920 x 1080 at 18 bpp and 24 bpp Color with Reduced Blanking
- ESD Rating ±2 kV

4.7 LED

The i.MX8MM-COMPACT-CM features a red LED controlled by GPIO4_IO27 signal of the i.MX8M-MINI. The LED is ON when GPIO4_IO27 is logic High.

5. Hirose DF40C connectors

The i.MX8MM-COMPACT-CM exposes two 100 pin Hirose connectors DF40C-100DP-0.4V(51).

Recommended mating connector for custom board interfacing with stacking height 1.5mm is DF40C-100DS-0.4V(51). With an appropriated mated connector stacking heights from 1.5mm up to 4mm are possible.

J1	Signal	i.MX8MM Ball	Default	Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
1	GPIO2_IO07	U26	gpio2.IO[7]	usdhc1.DATA5					gpio2.IO[7]
3	JTAG_TDI	E27							
5	JTAG_TDO	E26							
7	JTAG_TCK	F26							
9	JTAG_TMS	F27							
11	JTAG_TRST_B	C27							
13	BOOT_MODE1	G27							
15	BOOT_MODE0	G26							
17	GND								
19	SD2_nRST	AB26	gpio2.IO[19]	usdhc2.RESET_B					gpio2.IO[19]
21	SD2_nCD	AA26	gpio2.IO[12]	usdhc2.CD_B					gpio2.IO[12]
23	SD2_WP	AA27	gpio2.IO[20]	usdhc2.WP					gpio2.IO[20]
25	SD2_DATA2	V24	gpio2.IO[17]	usdhc2.DATA2					gpio2.IO[17]
27	SD2_DATA3	V23	gpio2.IO[18]	usdhc2.DATA3					gpio2.IO[18]
29	SD2_CLK	W23	gpio2.IO[13]	usdhc2.CLK					gpio2.IO[13]
31	SD2_CMD	W24	gpio2.IO[14]	usdhc2.CMD					gpio2.IO[14]
33	SD2_DATA1	AB24	gpio2.IO[16]	usdhc2.DATA1					gpio2.IO[16]
35	SD2_DATA0	AB23	gpio2.IO[15]	usdhc2.DATA0					gpio2.IO[15]
37	GPIO2_IO11	R24	gpio2.IO[11]	usdhc1.STROBE					gpio2.IO[11]
39	GPIO4_IO22	AB22	gpio4.IO[22]	sai2.RX_BCLK	sai5.TX_BCLK			uart1.RX	gpio4.IO[22]
41	SAI5_RXFS	AB15	gpio3.IO[19]	sai5.RX_SYNC	sai1.TX_DATA[0]				gpio3.IO[19]
43	SAI5_RXD0	AD18	gpio3.IO[21]	sai5.RX_DATA[0]	sai1.TX_DATA[2]			pdm.BIT_STREAM[0]	gpio3.IO[21]
45	SAI5_MCLK	AD15	gpio3.IO[25]	sai5.MCLK	sai1.TX_BCLK				gpio3.IO[25]
47	SAI5_RXC	AC15	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_BCLK			coresight.TRACE_CTL	gpio4.IO[1]
49	SAI5_RXD1	AC14	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[1]		pdm.BIT_STREAM[1]	coresight.TRACE[1]	gpio4.IO[3]
51	SAI5_RXD3	AC13	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[3]		pdm.BIT_STREAM[3]	coresight.TRACE[3]	gpio4.IO[5]
53	SAI5_RXD2	AD13	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[2]		pdm.BIT_STREAM[2]	coresight.TRACE[2]	gpio4.IO[4]
55	REF_CLK_32K	AG14	gpio1.IO[0]	gpio1.IO[0]	ccmsrcgpcmix.ENET_PHY_REF_CLK_ROOT				anamix.REF_CLK_32K
57	GPIO1_IO01	AF14	gpio1.IO[1]	gpio1.IO[1]	pwm1.OUT				anamix.REF_CLK_24M
59	GPIO1_IO06	AG11	gpio1.IO[6]	gpio1.IO[6]	enet1.MDC				usdhc1.CD_B
61	GPIO1_IO07	AF11	gpio1.IO[7]	gpio1.IO[7]	enet1.MDIO				usdhc1.WP
63	GND								
65	GPIO1_IO08	AG10	gpio1.IO[8]	gpio1.IO[8]	enet1.1588_EVENT0_IN				usdhc2.RESET_B
67	GPIO4_IO21	AC19	gpio4.IO[21]	sai2.RX_SYNC	sai5.TX_SYNC	sai5.TX_DATA[1]	sai2.RX_DATA[1]	uart1.TX	gpio4.IO[21]
69	ENET_LED_LINK100								
71	ENET_LED_LINK1000								
73	ENET_LED_ACT								
75	QSPIA_DATA2	K23	gpio3.IO[8]	rawnand.DATA02	qspi.A_DATA[2]	usdhc3.CD_B			gpio3.IO[8]
77	QSPIA_DATA1	K24	gpio3.IO[7]	rawnand.DATA01	qspi.A_DATA[1]				gpio3.IO[7]
79	QSPIA_nSS0	N24	gpio3.IO[1]	rawnand.CE0_B	qspi.A_SS0_B				gpio3.IO[1]
81	QSPIA_DATA3	N23	gpio3.IO[9]	rawnand.DATA03	qspi.A_DATA[3]	usdhc3.WP			gpio3.IO[9]
83	QSPIA_SCLK	N22	gpio3.IO[0]	rawnand.ALE	qspi.A_SCLK				gpio3.IO[0]
85	QSPIA_DATA0	P23	gpio3.IO[6]	rawnand.DATA00	qspi.A_DATA[0]				gpio3.IO[6]
87	SPDIF_RX	AG9	gpio5.IO[4]	spdif1.IN	pwm2.OUT				gpio5.IO[4]
89	SPDIF_TX	AF9	gpio5.IO[3]	spdif1.OUT	pwm3.OUT				gpio5.IO[3]
91	SPDIF_EXT_CLK	AF8	gpio5.IO[5]	spdif1.EXT_CLK	pwm1.OUT				gpio5.IO[5]
93	GPIO1_IO12	AB10	gpio1.IO[12]	gpio1.IO[12]	usb1.OTG_PWR				sdma2.EXT_EVENT[1]
95	GPIO1_IO14	AC9	gpio1.IO[14]	gpio1.IO[14]	usb2.OTG_PWR			usdhc3.CD_B	pwm3.OUT
97	GPIO1_IO13	AD9	gpio1.IO[13]	gpio1.IO[13]	usb1.OTG_OC				pwm2.OUT
99	GPIO1_IO15	AB9	gpio1.IO[15]	gpio1.IO[15]	usb2.OTG_OC			usdhc3.WP	pwm4.OUT

Figure 5.1: J1, odd pins

2	ENET_TX1_P								
4	ENET_TX1_N								
6	ENET_RX1_P								
8	ENET_RX1_N								
10	ENET_TX2_P								
12	ENET_TX2_N								
14	ENET_RX2_P								
16	ENET_RX2_N								
18	GND								
20	SAI1_TXD6	AG23	gpio4.IO[18]	sai1.TX_DATA[6]	sai6.RX_SYNC	sai6.TX_SYNC		coresight.TRACE[14]	gpio4.IO[18]
22	SAI1_TXD7	AF23	gpio4.IO[19]	sai1.TX_DATA[7]	sai6.MCLK		pdm.CLK	coresight.TRACE[15]	gpio4.IO[19]
24	SAI1_TXD4	AG22	gpio4.IO[16]	sai1.TX_DATA[4]	sai6.RX_BCLK	sai6.TX_BCLK		coresight.TRACE[12]	gpio4.IO[16]
26	SAI1_TXD5	AF22	gpio4.IO[17]	sai1.TX_DATA[5]	sai6.RX_DATA[0]	sai6.TX_DATA[0]		coresight.TRACE[13]	gpio4.IO[17]
28	SAI1_TXD2	AG21	gpio4.IO[14]	sai1.TX_DATA[2]	sai5.TX_DATA[2]			coresight.TRACE[10]	gpio4.IO[14]
30	SAI1_TXD3	AF21	gpio4.IO[15]	sai1.TX_DATA[3]	sai5.TX_DATA[3]			coresight.TRACE[11]	gpio4.IO[15]
32	SAI1_TXD1	AF20	gpio4.IO[13]	sai1.TX_DATA[1]	sai5.TX_DATA[1]			coresight.TRACE[9]	gpio4.IO[13]
34	SAI1_TXD0	AG20	gpio4.IO[12]	sai1.TX_DATA[0]	sai5.TX_DATA[0]			coresight.TRACE[8]	gpio4.IO[12]
36	SAI1_RXD6	AG19	gpio4.IO[8]	sai1.RX_DATA[6]	sai6.TX_SYNC	sai6.RX_SYNC		coresight.TRACE[6]	gpio4.IO[8]
38	SAI1_RXD7	AF19	gpio4.IO[9]	sai1.RX_DATA[7]	sai6.MCLK	sai1.TX_SYNC	sai1.TX_DATA[4]	coresight.TRACE[7]	gpio4.IO[9]
40	SAI1_RXD4	AG18	gpio4.IO[6]	sai1.RX_DATA[4]	sai6.TX_BCLK	sai6.RX_BCLK		coresight.TRACE[4]	gpio4.IO[6]
42	SAI1_RXD5	AF18	gpio4.IO[7]	sai1.RX_DATA[5]	sai6.TX_DATA[0]	sai6.RX_DATA[0]	sai1.RX_SYNC	coresight.TRACE[5]	gpio4.IO[7]
44	SAI1_RXD2	AG17	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[2]		pdm.BIT_STREAM[2]	coresight.TRACE[2]	gpio4.IO[4]
46	SAI1_RXD3	AF17	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[3]		pdm.BIT_STREAM[3]	coresight.TRACE[3]	gpio4.IO[5]
48	SAI1_RXFS	AG16	gpio4.IO[0]	sai1.RX_SYNC	sai5.RX_SYNC			coresight.TRACE_CLK	gpio4.IO[0]
50	SAI1_RXD0	AG15	gpio4.IO[2]	sai1.RX_DATA[0]	sai5.RX_DATA[0]	sai1.TX_DATA[1]	pdm.BIT_STREAM[0]	coresight.TRACE[0]	gpio4.IO[2]
52	SAI1_RXD1	AF15	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[1]		pdm.BIT_STREAM[1]	coresight.TRACE[1]	gpio4.IO[3]
54	SAI1_RXC	AF16	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_BCLK			coresight.TRACE_CTL	gpio4.IO[1]
56	SAI1_TXFS	AB19	gpio4.IO[10]	sai1.TX_SYNC	sai5.TX_SYNC			coresight.EVENTO	gpio4.IO[10]
58	SAI1_MCLK	AB18	gpio3.IO[25]	sai5.MCLK	sai1.TX_BCLK				gpio3.IO[25]
60	SAI1_TXC	AC18	gpio4.IO[11]	sai1.TX_BCLK	sai5.TX_BCLK			coresight.EVENTI	gpio4.IO[11]
62	GND								
64	GPIO1_IO05	AF12	gpio1.IO[5]	gpio1.IO[5]	m4.NMI				ccmsrcgpcmix.PMIC_READY
66	GPIO1_IO09	AF10	gpio1.IO[9]	gpio1.IO[9]	enet1.1588_EVENT0_OUT			usdhc3.RESET_B	sdma2.EXT_EVENT[0]
68	UART1_RXD	E14	gpio5.IO[22]	uart1.RX	ecspi3.SCLK				gpio5.IO[22]
70	UART1_TXD	F13	gpio5.IO[23]	uart1.TX	ecspi3.MOSI				gpio5.IO[23]
72	UART2_RXD	F15	gpio5.IO[24]	uart2.RX	ecspi3.MISO				gpio5.IO[24]
74	UART2_TXD	E15	gpio5.IO[25]	uart2.TX	ecspi3.SS0				gpio5.IO[25]
76	UART1_CTS	E18	gpio5.IO[26]	uart3.RX	uart1.CTS_B	usdhc3.RESET_B			gpio5.IO[26]
78	UART1_RTS	D18	gpio5.IO[27]	uart3.TX	uart1.RTS_B	usdhc3.VSELECT			gpio5.IO[27]
80	UART4_RXD	F19	gpio5.IO[28]	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]
82	UART4_TXD	F18	gpio5.IO[29]	uart4.TX	uart2.RTS_B				gpio5.IO[29]
84	I2C4_SDA	D13	gpio5.IO[21]	i2c4.SDA	pwm1.OUT				gpio5.IO[21]
86	I2C4_SCL	E13	gpio5.IO[20]	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]
88	GND								
90	SAI3_RXFS	AG8	gpio4.IO[28]	sai3.RX_SYNC	gpt1.CAPTURE1	sai5.RX_SYNC	sai3.RX_DATA[1]		gpio4.IO[28]
92	SAI3_RXD	AF7	gpio4.IO[30]	sai3.RX_DATA[0]	gpt1.COMPARE1	sai5.RX_DATA[0]		uart2.RTS_B	gpio4.IO[30]
94	SAI3_TXC	AG6	gpio5.IO[0]	sai3.TX_BCLK	gpt1.COMPARE2	sai5.RX_DATA[2]		uart2.TX	gpio5.IO[0]
96	SAI3_TXD	AF6	gpio5.IO[1]	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio5.IO[1]
98	SAI3_MCLK	AD6	gpio5.IO[2]	sai3.MCLK	pwm4.OUT	sai5.MCLK			gpio5.IO[2]
100	SAI3_TXFS	AC6	gpio4.IO[31]	sai3.TX_SYNC	gpt1.CLK	sai5.RX_DATA[1]	sai3.TX_DATA[1]	uart2.RX	gpio4.IO[31]

Figure 5.2: J1, even pins

SODIMM Pin	Signal	i.MX8MM Ball		Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
1	USB2_ID	D23							
3	USB2_VBUS	F23							
5	USB1_ID	D22							
7	USB1_VBUS	F22							
9	GND								
11	LVDS_CLK_N	B11	DSI_CLK_P						
13	LVDS_CLK_P	A11	DSI_CLK_N						
15	GND								
17	LVDS_TX3_N	B13	DSI_D3_P						
19	LVDS_TX3_P	A13	DSI_D3_N						
21	GND								
23	LVDS_TX2_N	B12	DSI_D2_P						
25	LVDS_TX2_P	A12	DSI_D2_N						
27	GND								
29	LVDS_TX1_N	B10	DSI_D1_P						
31	LVDS_TX1_P	A10	DSI_D1_N						
33	GND								
35	LVDS_TX0_N	B9	DSI_D0_P						
37	LVDS_TX0_P	A9	DSI_D0_N						
39	GND								
41	MX8_ONOFF	A25							
43	I2C1_SCL	E9	gpio5.IO[14]	i2c1.SCL	enet1.MDC				gpio5.IO[14]
45	I2C1_SDA	F9	gpio5.IO[15]	i2c1.SDA	enet1.MDIO				gpio5.IO[15]
47	POR_B	B24							
49	I2C3_SCL	E10	gpio5.IO[18]	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]
51	I2C3_SDA	D9	gpio5.IO[19]	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]
53	ECSPI2_MISO	A8	gpio5.IO[12]	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]
55	ECSPI2_MOSI	B8	gpio5.IO[11]	ecspi2.MOSI	uart4.TX				gpio5.IO[11]
57	ECSPI1_MISO	A7	gpio5.IO[8]	ecspi1.MISO	uart3.CTS_B				gpio5.IO[8]
59	ECSPI1_MOSI	B7	gpio5.IO[7]	ecspi1.MOSI	uart3.TX				gpio5.IO[7]
61	ECSPI1_SS0	B6	gpio5.IO[9]	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]
63	ECSPI2_SS0	A6	gpio5.IO[13]	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]
65	VDD_1V8								
67	VDD_1V8								
69	VDD_1V8								
71	VDD_3V3								
73	VDD_3V3								
75	VDD_3V3								
77	VSYS								
79	VSYS								
81	VSYS								
83	VSYS								
85	VSYS								
87	VSYS								
89	GND								
91	GND								
93	GND								
95	GND								
97	GND								
99	GND								

Figure 5.3: J2, odd pins

2	USB2_D_P	B23							
4	USB2_D_N	A23							
6	USB1_D_P	B22							
8	USB1_D_N	A22							
10	GND								
12	PCIE_REF_CLK_P	B21							
14	PCIE_REF_CLK_N	A21							
16	GND								
18	PCIE_TX_P	B20							
20	PCIE_TX_N	A20							
22	GND								
24	PCIE_RX_P	B19							
26	PCIE_RX_N	A19							
28	GND								
30	CSI_D3_P	B18							
32	CSI_D3_N	A18							
34	GND								
36	CSI_D2_P	B17							
38	CSI_D2_N	A17							
40	GND								
42	CSI_CLK_P	B16							
44	CSI_CLK_N	A16							
46	GND								
48	CSI_D1_P	B15							
50	CSI_D1_N	A15							
52	GND								
54	CSI_D0_P	B14							
56	CSI_D0_N	A14							
58	GND								
60	SYS_nRST								
62	ECSPI1_SCLK	D6	gpio5.IO[6]	ecspi1.SCLK	uart3.RX				gpio5.IO[6]
64	ECSPI2_SCLK	E6	gpio5.IO[10]	ecspi2.SCLK	uart4.RX				gpio5.IO[10]
66	VDD_1V8								
68	VDD_1V8								
70	VDD_1V8								
72	VDD_3V3								
74	VDD_3V3								
76	VDD_3V3								
78	VSYS								
80	VSYS								
82	VSYS								
84	VSYS								
86	VSYS								
88	VSYS								
90	GND								
92	GND								
94	GND								
96	GND								
98	GND								
100	GND								

Figure 5.4: J2, even pins

6. CPU Module interfaces

6.1 Display interfaces

i.MX8MM-COMPACT-CM provides the following display interfaces:

- MIPI DSI

  The MIPI-DSI interface is based on the four-lane MIPI display interface available with the iMX8M-MINI SoC. The DSI signals are available on the HIROSE DF40C connector if the SN65DSI83 is not assembled.

  The following main features are supported:

  - Up to 4 data lanes support D-PHY

- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)
- Supports High Speed and Low Power operation
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

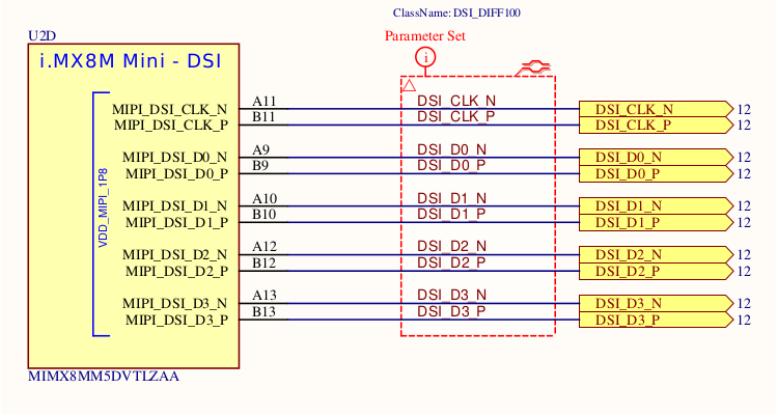


Figure 6.1: MIPI-DSI

- LVDS Interface (optional) – using Texas Instruments SN65DSI83 MIPI-DSI to LVDS bridge. If not assembled, then all DSI signals are available on the HIROSE DF40C connector. Texas Instruments SN65DSI83 supports following main features:
  - LVDS Output Clock Range of 25 MHz to 154MHz.
  - Suitable for up to 60 fps WUXGA 1920 x 1080 at 18 bpp and 24 bpp Color with Reduced Blanking
  - Capable of supporting the full resolution of the iMX8M MIPI-DSI interface with reduced blanking
  - ESD Rating ±2 kV

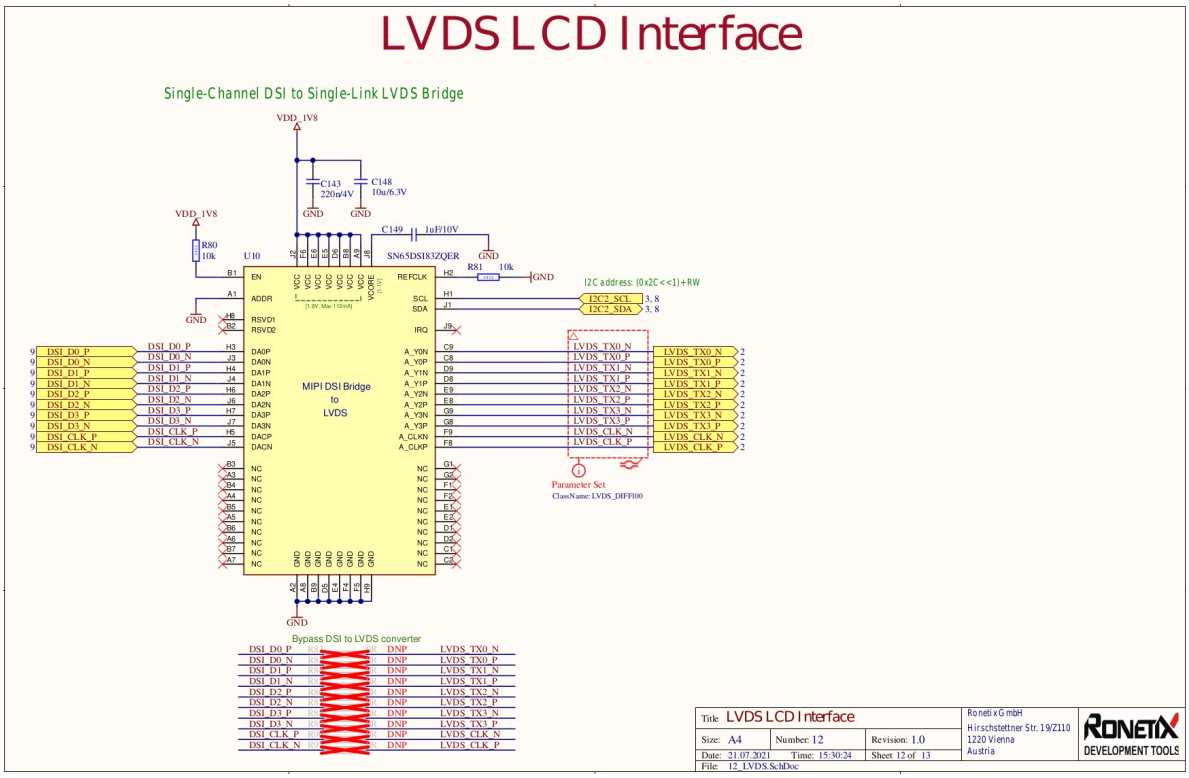


Figure 6.2: LVDS Interface

6.2 MIPI-CSI Camera interface

i.MX8MM-COMPACT-CM MIPI-CSI interface is derived from the four-lane MIPI-CSI host controller (MIPI_CSI) integrated into the iMX8M-MINI SoC. The CSI1 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-1 specification, providing an interface between i.MX8MM-COMPACT-CM and a MIPI CSI-1 compliant camera sensor. The following main features are supported:

- Up-to four data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Compliant with MIPI D-PHY standard specification V1.1 and Samsung D-PHY.
- Supports unidirectional Master operation
- Supports high speed mode (80Mbps - 1.5Gbps) per lane, providing 4K@30fps capability for the 4 lanes
- Support 5M pixel at 15 fps, 1080p30, 720p60, VGA at 60 fps
- Support for all CSI-2 data types:

- RGB444, RGB555, RGB565, RGB666, RGB888
- Legacy YUV420 8 bit
- RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- User Defined Data Types

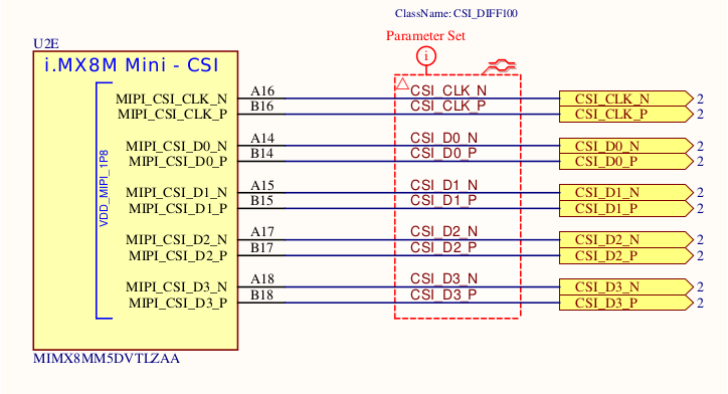


Figure 6.3: MIPI-CSI

6.3 USB interface

The i.MX8M-MINI SoC is equipped with two USB OTG controllers and PHYs. Each USB instance contains a USB 2.0 core. Both ports support dual-role functionality. The USB ports support the following main features:

- High-Speed/Full-Speed/Low-Speed OTG core
- Hardware support for OTG signaling, Session Request Protocol (SRP), Host Negotiation Protocol (HNP), and Attach Detection Protocol (ADP). ADP support includes dedicated timer hardware and register interface
- up to 8 endpoints
- Core0 supports charger detection with register interface only
- Low-power mode with local and remote wake-up capability

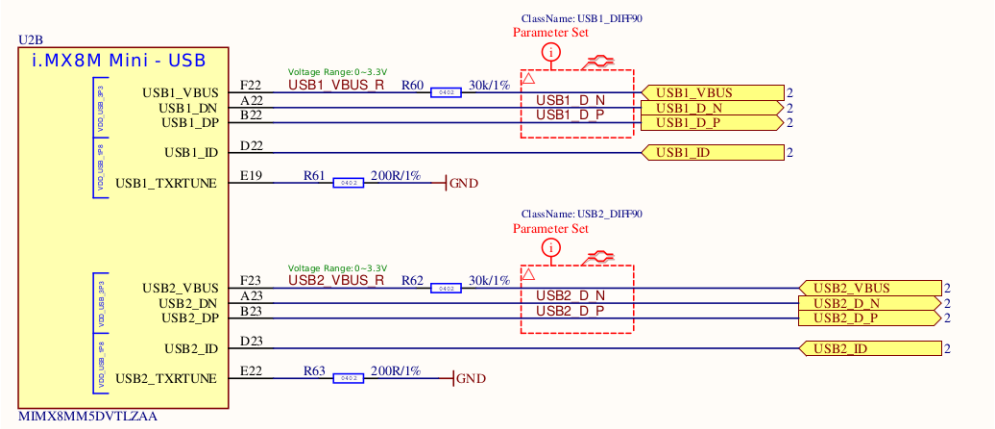


Figure 6.4: USB

6.4 PCI-Express

The i.MX8M-MINI SoC is equipped with one single lane PCI Express port (PCIe) Gen 2. The PCI Express ports support the following main features:

- Dual mode (DM) controller provides a solution to implement a PCI Express port for a PCI Express root complex or endpoint application.
- Port solution includes the controller (an analog PHY macro) and application logic to source and sink data.
- PCI Express base specification 2.0 with maximum 5.0Gbps lane rate.
- Native PCIe PM Mechanisms

Following standards are implemented:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PIPE Specification for PCI Express, Version 4.3, Intel Corporation
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2

On i.MX8MM-COMPACT-CM SoM PCIe is connected to the Hirose DF40C connector and requires an external 100MHz PCIe compliant reference clock.

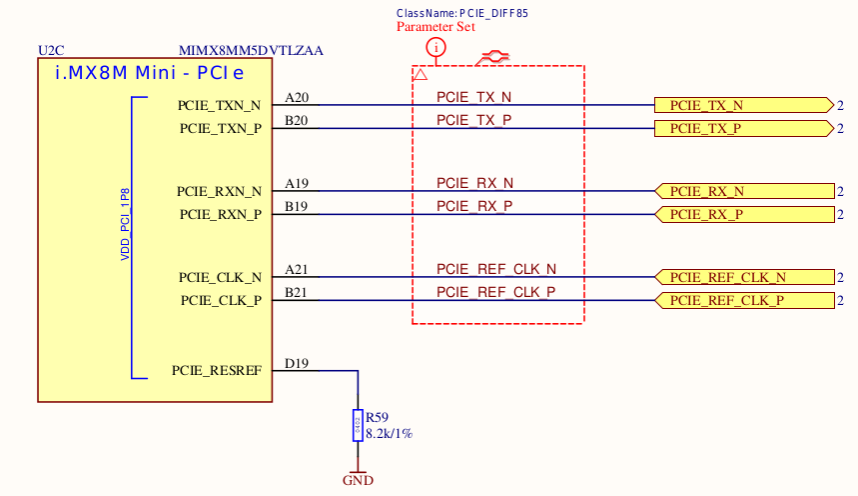


Figure 6.5: PCIe

6.5 MMC, SD, SDIO

The i.MX8M-MINI SoC is equipped with three MMC/SD/SDIO controller IPs (uSDHC). On i.MX8MM-COMPACT-CM SD3 is connected to the eMMC, SD1 is connected to the WiFi module, SD2 is available on the Hirose DF40C connector.

The uSDHC supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- Dedicated “card detection” and “write protection” signals
- Both 1.8V and 3.3V signaling support (uSDHC port 1 with 1-bit and 4-bit operation modes only).

6.6 UART

The i.MX8MM-COMPACT-CM exposes up to 4 UART interfaces some of which are multiplexed with other peripherals.

The i.MX8M-MINI UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible
- 9-bit or Multidrop mode (RS-485) support
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with capability to wake the processor from STOP mode through an on-chip interrupt.

6.7 I2C

The i.MX8M-MINI SoC is equipped with four I2C bus interfaces. I2C1, I2C3 and I2C4 are available on the Hirose DF40C connector. I2C2 is used internally, not available on Hirose DF40C. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

I2C usage table:

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1 1.8V	i.MX8MM-COMPACT-MB: Camera on CSI1	(0x3C<<1)+RW
	i.MX8MM-COMPACT-MB: RTC clock, 3.3V*	(0x50<<1)+RW
	i.MX8MM-COMPACT-MB: Audio Codec, 3.3V*	(0x34<<1)+RW
	i.MX8MM-COMPACT-MB: miniPCIEe Ref. Clock	(0x6A<<1)+RW
I2C2 1.8V only on CM	i.MX8Mx-COMPACT-CM: PMIC control	(0x4B<<1)+RW
	i.MX8Mx-COMPACT-CM: LVDS	(0x2C<<1)+RW
I2C3 1.8V	i.MX8MM-COMPACT-MB: PCIe M.2	

Note: 3.3V* - through voltage translator

Figure 6.6: I2C address usage

6.8 SPI

Up-to three SPI interfaces are accessible through the i.MX8MM-COMPACT-CM base board interface. The SPI interfaces are derived from i.MX8M-MINI integrated synchronous serial interface (eCSPI). Each instance of eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

6.9 Quad SPI

QSPI-A signals are available on Hirose DF40C connector.

The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- DMA support.
- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

6.10 PWM

Up to four PWM output signals are available at the i.MX8MM-COMPACT-CM base board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

6.11 GPIO

Up-to 89 of the i.MX8M-MINI general purpose input/output (GPIO) signals are available on the Hirose DF40C connector. When configured as an output, it is possible to write to an i.MX8M-MINI register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M-MINI register. In addition GPIOs peripheral can produce interrupts.

6.12 JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG signals are available on the Hirose DF40C connector.

7. Power Supply

7.1 Power supply from base board

i.MX8MM-COMPACT-CM is powered by regulated DC supply 3.85-5.0V

Signal	Type	Description
VIN_4V2	Power input	Main Power Supply 3.85-5.0V
GND	Power input	Common ground

7.2 Power supply provided to base board

i.MX8MM-COMPACT-CM provides 1.8V and 3.3V power supplies to the Hirose DF40C connector.

Signal	Type	Description
VDD_1V8	Power output	1.8V, Max. 0.5A
VDD_3V3	Power output	3.3V, Max. 1.5A

7.3 System Signals

Signal	Type	Description
MX8_ONOFF	Input with Pull-Up resistor	ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
SYS_nRST	Input	PMIC Power On signal

8. Electrical Specifications

8.1 Absolute maximum ratings

Parameter	MIn	Max	Unit
VIN_4V2 – Main Power Supply	-0.3	5.25	V
USB_VBUS - USB_HOST_VBUS, USB_OTG_VBUS	-0.3	5.25	V

8.2 Recommended Operating Conditions

Parameter	MIn	Typ	Max	Unit
VIN_4V2 – Main Power Supply	3.8	4.2	5.0	V
VIN_4V2 – recommended source capability		4.0		A

9. Operating Temperature Ranges

Range	Temp.
Commercial	0° to +70°C
Industrial	-40° to +85°C

10. Cooling

A cooling solution should be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the iMX8MM-COMPACT-CM temperature specifications.

11. Mechanical Drawings

All dimensions are in millimeters.

The height of all parts is < 2mm.

The base board connector provides 1.5mm board to board clearance.

Board thickness is 1.0mm

11.1 Base board mounting

i.MX8MM-COMPACT-CM SoM has two mounting quarter-holes for mounting to the base board which are plated and connected to GND.

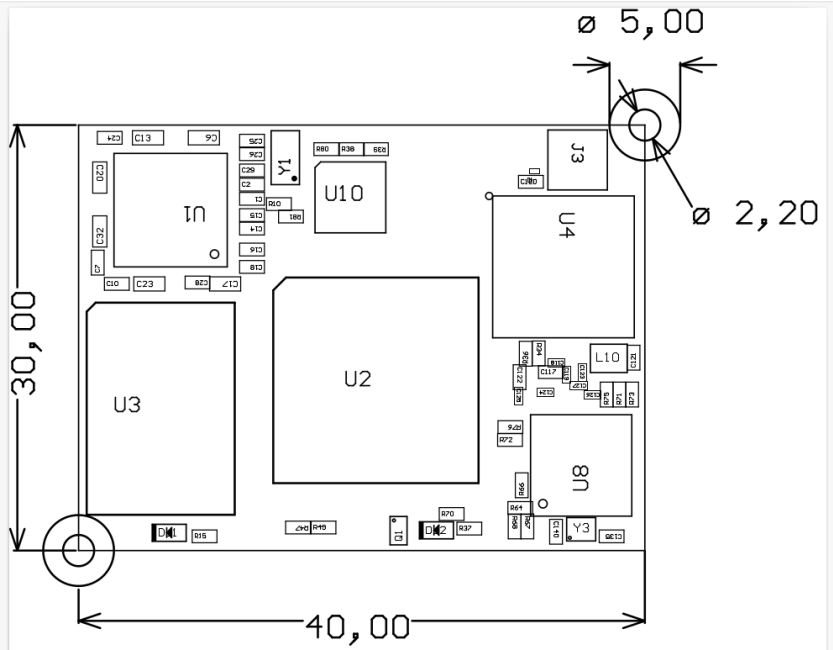


Figure 11.1: Assembly drawing

11.2 Standoffs

Fix i.MX8MM-COMACT-CM to the base board by mounting two spacers with suitable screws. The spacers should be:

- M2x0.4, length 1.5mm

12. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix's sole liability shall be for Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

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