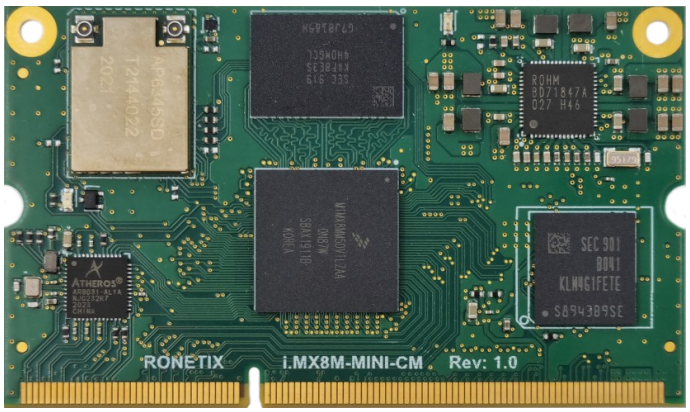
RONETIX
DEVELOPMENT TOOLS

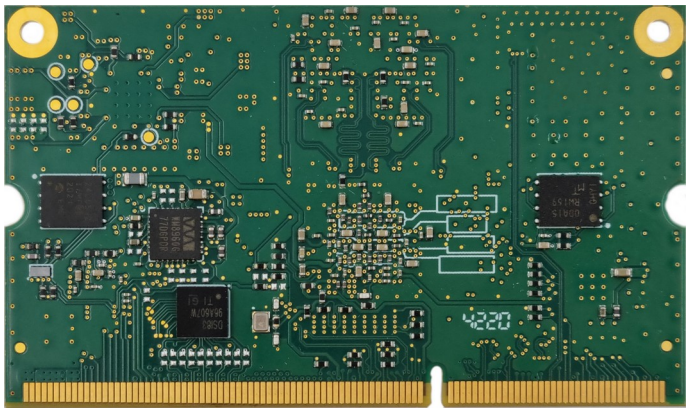
i.MX8M-NANO-CM

CPU Module (SoM) with NXP i.MX8M-NANO

Datasheet

rev 1.0





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1. Document Revision History

Revision	Date	Notes
1.0	15-Sep-2021	Initial release

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3. Overview

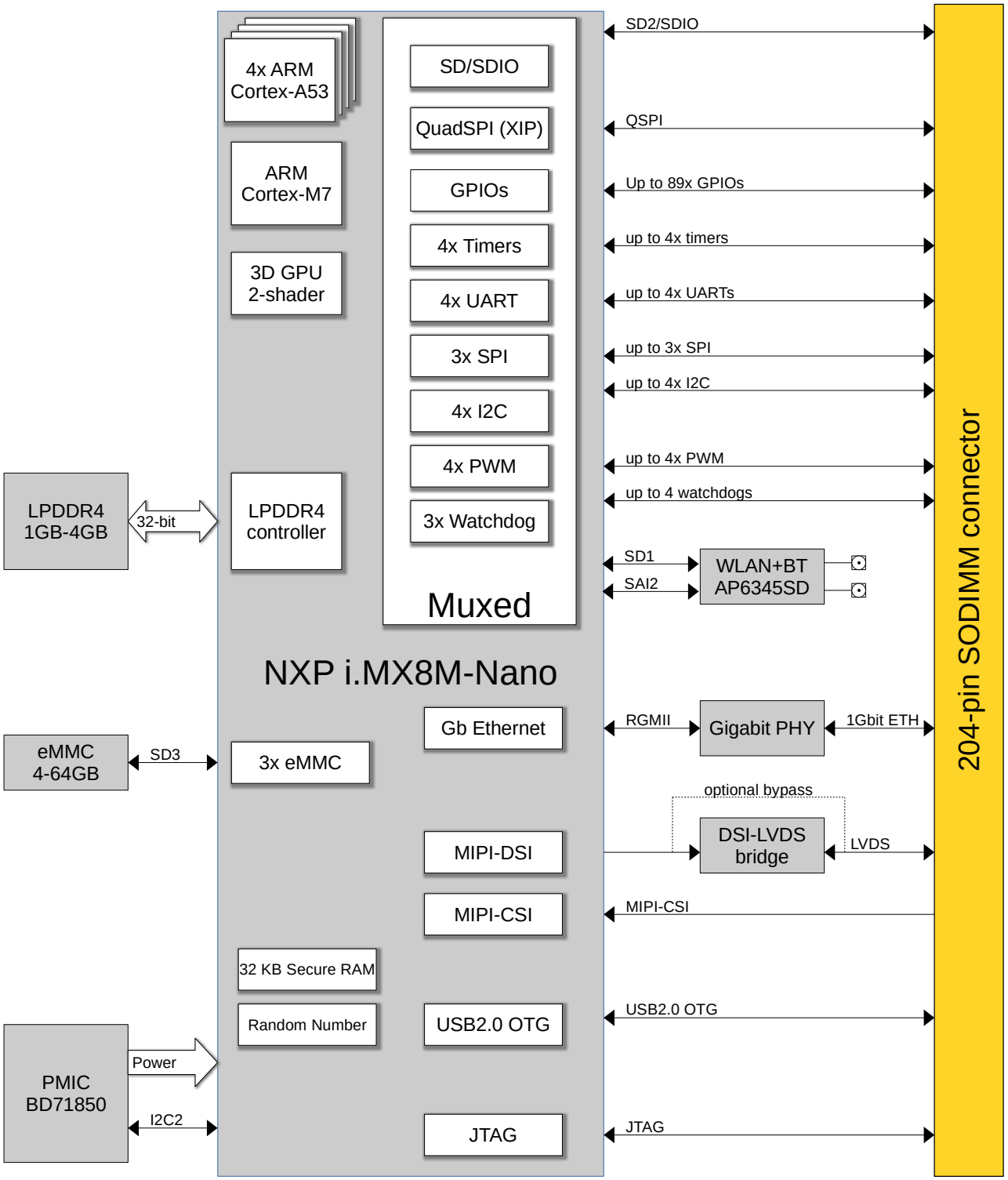
3.1 General Information

The **i.MX8M-NANO-CM** is a high-performance processing for low-power CPU Module (SoM – System On Module) that perfectly fits various embedded products of connected and portable devices. It is based on the NXP i.MX8M-Nano family of multipurpose processors from which feature a quad ARM® Cortex™-A53 up to 2GHz + an additional ARM Cortex-M7. This Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux on the Cortex-A53 core and an RTOS like FreeRTOS™ on the Cortex-M7 core for time and security critical tasks.

3.2 Highlights

CPU	• Quad/Duo/Solo Armv8-A, 64-bit Cortex™-A53 Core, 1.5GHz • ARM® Cortex™-M7, 750MHz
Memory	• RAM: 1 GiB LPDDR4 (optional: up to 4 GiB) • eMMC: 4 GiB (optional: up to 64 GiB)
Display	• LVDS, up to 1400 x 1050 @60Hz • MIPI DSI
Camera	• MIPI-CSI, 4 data lanes
Network	• Ethernet: 10/100/1000Mbps • WiFi: SparkLAN AP6345SD, 802.11ac, dual band (optional) • Bluetooth: Bluetooth 5.0 (optional)
I/O	• USB2.0 OTG port • Up to 4x UART ports • MMC/SD/SDIO • Up to 3x SPI • Up to 4x I2C • Up to 4x general purpose PWM signals • GPIOs
Electrical	• Supply Voltage: 3.85 – 5.0V
Physical	• Board size: 67x40mm • SO-DIMM 200 JEDEC MO-274 module (67.6x40mm) • Operation temperature: 0° +70°C, -20° to 85° C (optional) • Relative humidity: 10% to 90%

3.3 SoM Block Diagram


4x ARM Cortex-A53
ARM Cortex-M7
3D GPU 2-shader
SD/SDIO
QuadSPI (XIP)
GPIOs
4x Timers
4x UART
3x SPI
4x I2C
4x PWM
3x Watchdog
Muxed
NXP i.MX8M-Nano
LPDDR4 1GB-4GB
32-bit
LPDDR4 controller
eMMC 4-64GB
SD3
3x eMMC
Gb Ethernet
MIPI-DSI
MIPI-CSI
32 KB Secure RAM
Random Number
USB2.0 OTG
JTAG
PMIC BD71850
Power
I2C2
SD2/SDIO
QSPI
Up to 89x GPIOs
up to 4x timers
up to 4x UARTs
up to 3x SPI
up to 4x I2C
up to 4x PWM
up to 4 watchdogs
SD1
SAI2
WLAN+BT AP6345SD
RGMII
Gigabit PHY
1Gbit ETH
optional bypass
DSI-LVDS bridge
LVDS
MIPI-CSI
USB2.0 OTG
JTAG
204-pin SODIMM connector

4. CPU Module Hardware Components

This chapter describes the hardware components of i.MX8M-NANO-CM SoM.

4.1 Power supply

i.MX8M-NANO-CM uses Rohm's BD71850 as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8M series of application processors. The PMIC regulates all power rails required on CPU module from a single 3.85V-5.0V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

4.2 CPU i.MX8M-NANO

The i.MX 8M-NANO Dual / 8M Quad processors represent NXP's latest market of connected streaming audio/video devices, scanning/imaging devices, and various devices requiring high-performance, low-power processors. The i.MX 8M-NANO Dual / 8M Quad processors feature advanced implementation of a quad Arm®Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general purpose Cortex®-M7 core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3Lmemory. There are a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

4.2.1 CPU Block Diagram

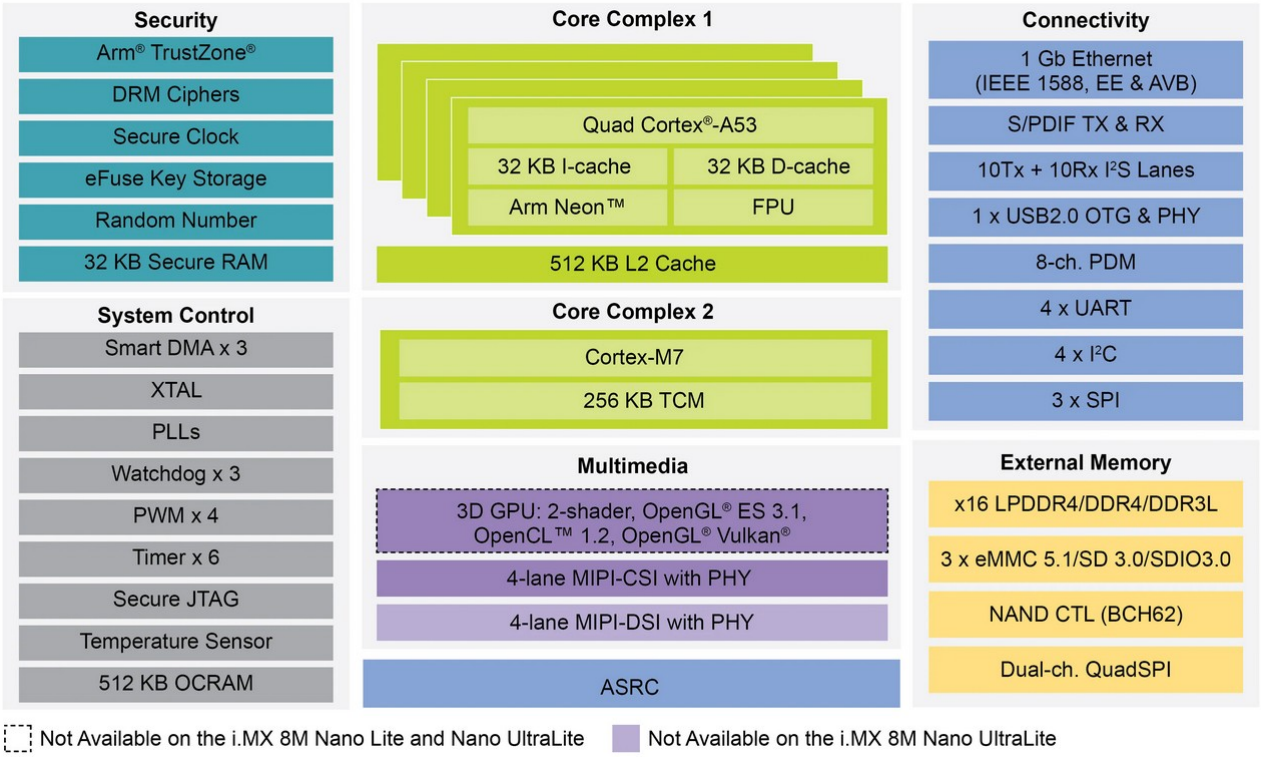


Figure 4.1: CPU Block diagram

4.2.2 CPU Platform

The i.MX8M-NANO processor implements up to four ARM® Cortex®-A53 cores intended for high level O/S, with an ARM® Cortex®-M7 core dedicated for real-time tasks.

The ARM Cortex-A53 MPCore™ platform has the following features:

- Quad ARM Cortex-A53 Cores
- Target frequency of 1.5GHz
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - MPE (media processing engine) with NEON co-processor supporting SIMD architecture

- The Arm Cortex-A53 Core complex shares:
  - General interrupt controller (GIC) with 128 interrupt support
  - Global timer
  - Snoop control unit (SCU)
  - 1 MB unified I/D L2 cache
  - NEON MPE co-processor
    - SIMD Media Processing Architecture
    - NEON register file with 32x64-bit general-purpose registers
    - NEON Integer execute pipeline (ALU, Shift, MAC)
    - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
    - NEON load/store and permute pipeline

The ARM Cortex-M7 platform includes the following features:

- Cortex-M7 CPU core operating at 750 MHz
- MPU (memory protection unit)
- FPU (floating-point unit)
- 32 KByte instruction cache
- 32 KByte data cache
- 256 KByte TCM (tightly-coupled memory)

4.3 Memory

4.3.1 DRAM

i.MX8M-NANO-CM is standard equipped with 1 GB LPDDR4 memory. Optionally up to 4 GB can be assembled. The data bus is 32-bit wide.

4.3.2 eMMC – non-volatile storage memory

i.MX8M-NANO-CM is standard equipped with 4 GB eMMC. Optionally up to 32 GB can be assembled.

The eMMC can be used as boot device.

4.4 SPI NOR Flash

i.MX8M-NANO-CM can be assembled with a QSPI NOR Flash.

4.5 I2C EEPROM

i.MX8M-NANO-CM can be assembled with an I2C EEPROM.

4.6 Gigabit Ethernet

i.MX8M-NANO-CM implements one full-featured 10/100/1000 Ethernet ports implemented with MAC built into the i.MX8M-NANO SoC, coupled with AR8031 RGMII Ethernet PHYs from Qualcomm. The Ethernet interface support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

4.7 WLAN

i.MX8M-NANO-CM optional wireless communication is implemented with SparkLAN AP6345SD WLAN module. AP6345SD is an 802.11ac/b/g/n Dual-Band Wi-Fi+Bluetooth module based on Cypress's BCM43456 chipset. It is Dual-Band AC on 2.4GHz + 5GHz and incorporates Bluetooth 5.0. The download speed are 300Mbps on N networks and 867Mbps on AC network.

i.MX8M-NANO-CM is equipped with two U.FL high frequency connectors for external antennas.

4.8 Audio

i.MX8M-NANO-CM implements an audio codec WM8960 (assembled optional) . The WM8960 is a low power stereo codec featuring Class D speaker drivers to provide 1W per channel into 8Ω loads. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required. Advanced on-chip digital signal processing performs automatic level control for the microphone or line input. Stereo 24-bit Delta Sigma converters are used with low power over-sampling digital interpolation and decimation filters and a flexible

digital audio interface. The main clock can be input directly or generated internally by an onboard PLL, supporting most commonly used clocking schemes.

The WM8960 supports the following features:

- Stereo class D speaker driver, 1W per channel
- On-chip headphone driver 40mW output power into 16Ω
- Microphone interface
- Pop and click suppression
- DAC SNR 98 dB ('A' weighted), THD -84 dB at 48 kHz, 3.3V
- ADC SNR 95 dB ('A' weighted),THD -82 dB at 48 kHz, 3.3V
- Programmable ALC / limiter and noise gate

Please refer to the WM8960 datasheet for additional details.

4.9 LVDS bridge

i.MX8M-NANO-CM implements (optional) onboard LVDS display interface by converting the MIPI-DSI to LVDS signals using Texas Instruments SN65DSI83 transceiver. The SN65DSI83 DSI to FlatLink bridge device features a single-channel MIPI D-PHY receiver front-end configuration with four lanes per channel operating at 1 Gbps per lane; a maximum input bandwidth of 4 Gbps. The bridge decodes MIPI DSI18 bpp RGB666 and 24 bpp RGB888 packets and converts the formatted video data stream to a FlatLink compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Single-Link LVDS with four data lanes per link. The SN65DSI83 device can support up to WUXGA1920 × 1200 at 60 frames per second, at 24 bpp with reduced blanking. The SN65DSI83 device is also suitable for applications using 60 fps 1366 × 768 /1280 × 800 at 18 bpp and 24 bpp. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces. Designed with industry-compliant interface technology, the SN65DSI83 device is compatible with a wide range of microprocessors, and is designed with a range of power management features including low-swing LVDS outputs, and the MIPI defined ultra-low power state (ULPS) support.

Main features:

- LVDS Output Clock Range of 25 MHz to 154MHz.
- Suitable for up to 60 fps WUXGA 1920 x 1080 at 18 bpp and 24 bpp Color with Reduced Blanking
- ESD Rating ±2 kV

4.10 LED

The i.MX8M-NANO-CM features a red LED controlled by GPIO4_IO27 signal of the i.MX8M-NANO. The LED is ON when GPIO4_IO27 is logic High.

5. SODIMM204 connector

The i.MX8M-NANO-CM exposes a 204 pin SO-DIMM connector.

Recommended mating Connector socket for custom board interfacing are the following connectors (or equivalent):

- TE Connectivity 2013289-2 or 2013289-1
- Cvilux CS69-2042CA0-R0
- JAE MM80-204B1-1

SODIMM Pin	Signal	i.MX8M Ball	Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
1	ETH1_TX1_P							
3	ETH1_TX1_N							
5	ETH1_RX1_P							
7	ETH1_RX1_N							
9	ETH1_TX2_P							
11	ETH1_TX2_N							
13	ETH1_RX2_P							
15	ETH1_RX2_N							
17	ETH1_LED_ACT							
19	ETH1_LED_LINK100							
21	SD2_nCD	AA26	usdhc2.CD_B					gpio2.IO[12]
23	ETH1_LED_LINK1000							
25	GPIO2_IO07	U26	usdhc1.DATA5					
27	GPIO1_IO09	AF10	gpio1.IO[9]				usdhc3.RESET_B	
29								
31								
33								
35								
37								
39								
41		A21						
43		B21						
45		A20						
47		B20						
49		A19						
51		B19						
53	CSI1_D0_P	B14						
55	CSI1_D0_N	A14						
57	CSI1_CLK_P	B16						
59	CSI1_CLK_N	A16						
61								
63								
65								
67								
69								
71								
73	USB1_VBUS	F22						
75	USB1_ID	D22						
77	USB1_D_P	B22						
79	USB1_D_N	A22						
81								
83								
85								
87								
89		B23						
91		A23						
93								
95								
97								
99								
101		F23						
103		D23						
105	I2C4_SDA	E13	I2C4_SDA	pwm1.OUT				gpio5.IO[21]
107	UART2_TXD	E15	uart2.TX	ecspi3.SS0				gpio5.IO[25]
109	UART1_RTS	D18	uart3.TX	uart1.RTS_B	usdhc3.VSELECT			gpio5.IO[27]
111	UART1_CTS	E18	uart3.RX	uart1.CTS_B	usdhc3.RESET_B			gpio5.IO[26]
113	UART4_RXD	F19	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]
115	ECSPI2_SS0	A6	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]
117	ECSPI2_MISO	A8	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]
119	ECSPI1_MOSI	B7	ecspi1.MOSI	uart3.TX				gpio5.IO[7]
121	UART3_CTS	A7	ecspi1.MISO	uart3.CTS_B				gpio5.IO[8]
123		AB18						
125		AG23						
127		AG21						
129		AF22						
131		AF23						
133		AG22						
135		AF21						
137		AF20						
139		AC18						
141		AG20						
143		AF18						
145		AG19						
147		AF19						
149		AG17						
151		AB19						
153		AF17						
155		AG18						
157		AG15						
159		AF16						
161		AF15						
163		AG16						
165	MIC							
167	GND							
169	UART2_RXD	E15	uart2.RX	ecspi3.MISO				gpio5.IO[24]
171	UART4_TXD	F18	uart4.TX	uart2.RTS_B				gpio5.IO[29]
173	ECSPI1_SCLK	D6	ecspi1.SCLK	uart3.RX				gpio5.IO[6]
175	ECSPI2_SCLK	E6	ecspi2.SCLK	uart4.RX				gpio5.IO[10]
177	ECSPI2_MOSI	B8	ecspi2.MOSI	uart4.TX				gpio5.IO[11]
179	UART3_RTS	B6	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]
181	UART1_RXD	E14	uart1.RX	ecspi3.SCLK				gpio5.IO[22]
183	UART1_TXD	F13	uart1.TX	ecspi3.MOSI				gpio5.IO[23]
185	SYS_nRST							
187	VDD_1V8							
189	VDD_1V8							
191	YSYS							
193	YSYS							
195	YSYS							
197	YSYS							
199	YSYS							
201	GND							
203	GND							

Figure 5.1: J1, odd pins

SODIMM Pin	Signal	i.MX8M Ball	Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
2	GND							
4	MX8_ONOFF	A25						
6	GPIO1_IO14	AC9						
8	BOOT_MODE1	G27						
10	BOOT_MODE0	G26						
12	PCIe_nRST	AC19						
14	TCPC_nINT	R24	usdhc1.STROBE					gpio2.IO[11]
16	GPIO1_IO05	AF12	gpio1.IO[5]					
18	SD2_nRST	AB26	usdhc2.RESET_B					gpio2.IO[19]
20	SD2_DATA2	V24	usdhc2.DATA2					gpio2.IO[17]
22	GND							
24	SD2_DATA1	AB24	usdhc2.DATA1					gpio2.IO[16]
26	SD2_DATA0	AB23	usdhc2.DATA0					gpio2.IO[15]
28	SD2_DATA3	V23	usdhc2.DATA3					gpio2.IO[18]
30	SD2_WP	AA27	usdhc2.WP					gpio2.IO[20]
32	SD2_CMD	W24	usdhc2.CMD					gpio2.IO[14]
34	SD2_CLK	W23	usdhc2.CLK					gpio2.IO[13]
36	GPIO2_IO8	W27	usdhc1.DATA6					gpio2.IO[8]
38	BT_USB_D_N							
40	BT_USB_D_P							
42	CLKO2	AB9	gpio1.IO[15]	usb2.OTG_OC			usdhc3.WP	pwm4.OUT
44	GND							
46	GPIO1_IO12	AB10	gpio1.IO[12]	usb1.OTG_PWR				
48	SPDIF_TX	AF9						
50	SPDIF_RX	AG9						
52	CSI1_D2_N	A17						
54	CSI1_D2_P	B17						
56	CSI1_D1_P	B15						
58	CSI1_D1_N	A15						
60	CSI1_D3_P	B18						
62	CSI1_D3_N	A18						
64								
66								
68								
70								
72	GND							
74	GPIO1_IO13	AD9	gpio1.IO[13]	usb1.OTG_OC				pwm2.OUT
76	SAI5_MCLK	AD15	sai5.MCLK	sai1.TX_BCLK				gpio3.IO[25]
78	SAI5_RXD3	AC13	sai5.RX_DATA[3]	sai1.TX_DATA[5]	sai1.TX_SYNC	sai5.TX_DATA[0]		gpio3.IO[24]
80	SAI5_RXD1	AC14	sai5.RX_DATA[1]	sai1.TX_DATA[3]	sai1.TX_SYNC	sai5.TX_SYNC		gpio3.IO[22]
82	SAI5_RXC	AC15	sai5.RX_BCLK	sai1.TX_DATA[1]				gpio3.IO[20]
84	I2C1_SDA	F9	i2c1.SDA	enet1.MDIO				gpio5.IO[15]
86	I2C1_SCL	E9	i2c1.SCL	enet1.MDC				gpio5.IO[14]
88	I2C3_SDA	F10	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]
90	SPDIF_EXT_CLK	AF8						
92	I2C4_SCL	D13	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]
94	I2C3_SCL	E10	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]
96	GND							
98	SAI5_RXD2	AD13	sai5.RX_DATA[2]	sai1.TX_DATA[4]	sai1.TX_SYNC	sai5.TX_BCLK		gpio3.IO[23]
100	SAI5_RXD0	AD18	sai5.RX_DATA[0]	sai1.TX_DATA[2]				gpio3.IO[21]
102	GPIO1_IO08	AG10	gpio1.IO[8]					
104	SAI5_RXFS	AB15	sai5.RX_SYNC	sai1.TX_DATA[0]				gpio3.IO[19]
106								
108								
110								
112								
114								
116								
118								
120								
122								
124								
126								
128								
130								
132								
134	GND							
136	LVDS0_TX0_N							
138	LVDS0_TX0_P							
140	LVDS0_TX1_N							
142	LVDS0_TX1_P							
144	LVDS0_TX2_N							
146	LVDS0_TX2_P							
148	LVDS0_CLK_N							
150	LVDS0_CLK_P							
152	LVDS0_TX3_N							
154	LVDS0_TX3_P							
156	SAI2_RXC	AB22	sai2.RX_BCLK	sai5.TX_BCLK			uart1.RX	gpio4.IO[22]
158	HEADPHONE_R							
160	HEADPHONE_L							
162	SAI3_MCLK	AD6	sai3.MCLK	pwm4.OUT	sai5.MCLK			gpio5.IO[2]
164	SPK_RP							
166	SPK_RN							
168	GND							
170	JTAG_TCK	F26						
172	JTAG_TMS	F27						
174	JTAG_TRST_B	C27						
176	JTAG_TDO	E26						
178	JTAG_TDI	E27						
180	GPIO1_IO01	AF14	gpio1.IO[1]	pwm1.OUT				
182	GPIO1_IO07	AF11	gpio1.IO[7]					
184	CSI_nRST	AG11	gpio1.IO[6]					
186	GPIO2_IO9	W26	usdhc1.DATA7					gpio2.IO[9]
188	VDD_1V8							
190	VDD_1V8							
192	YSYS							
194	YSYS							
196	YSYS							
198	YSYS							
200	YSYS							
202	GND							
204	GND							

Figure 5.2: J1, even pins

6. CPU Module interfaces

6.1 Display interfaces

i.MX8M-NANO-CM provides the following display interfaces:

- MIPI DSI

  The MIPI-DSI interface is based on the four-lane MIPI display interface available with the iMX8M-NANO SoC. The DSI signals are available on the SODIMM204 connector if the SN65DSI83 is not assembled.

  The following main features are supported:

  - Up to 4 data lanes support D-PHY
  - Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
  - Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)
  - Supports High Speed and Low Power operation
  - MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

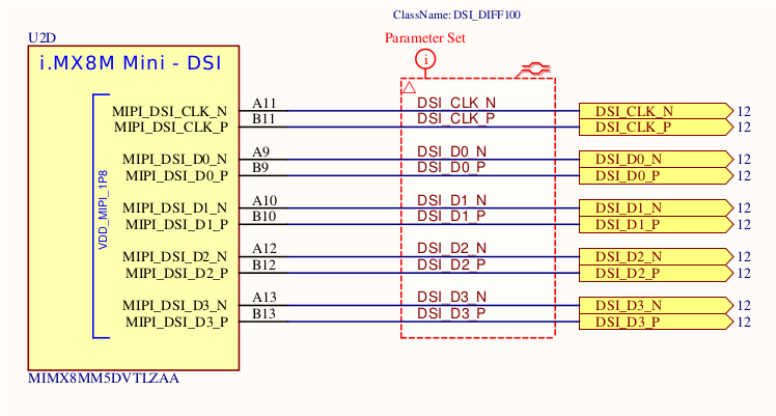


Figure 6.1: MIPI-DSI

- LVDS Interface (optional) – using Texas Instruments SN65DSI83 MIPI-DSI to LVDS bridge. If not assembled, then all DSI signals are available on the SODIMM204 connector. Texas Instruments SN65DSI83 supports following main features:

  - LVDS Output Clock Range of 25 MHz to 154MHz.

- Suitable for up to 60 fps WUXGA 1920 x 1080 at 18 bpp and 24 bpp Color with Reduced Blanking
- Capable of supporting the full resolution of the iMX8M MIPI-DSI interface with reduced blanking
- ESD Rating ±2 kV

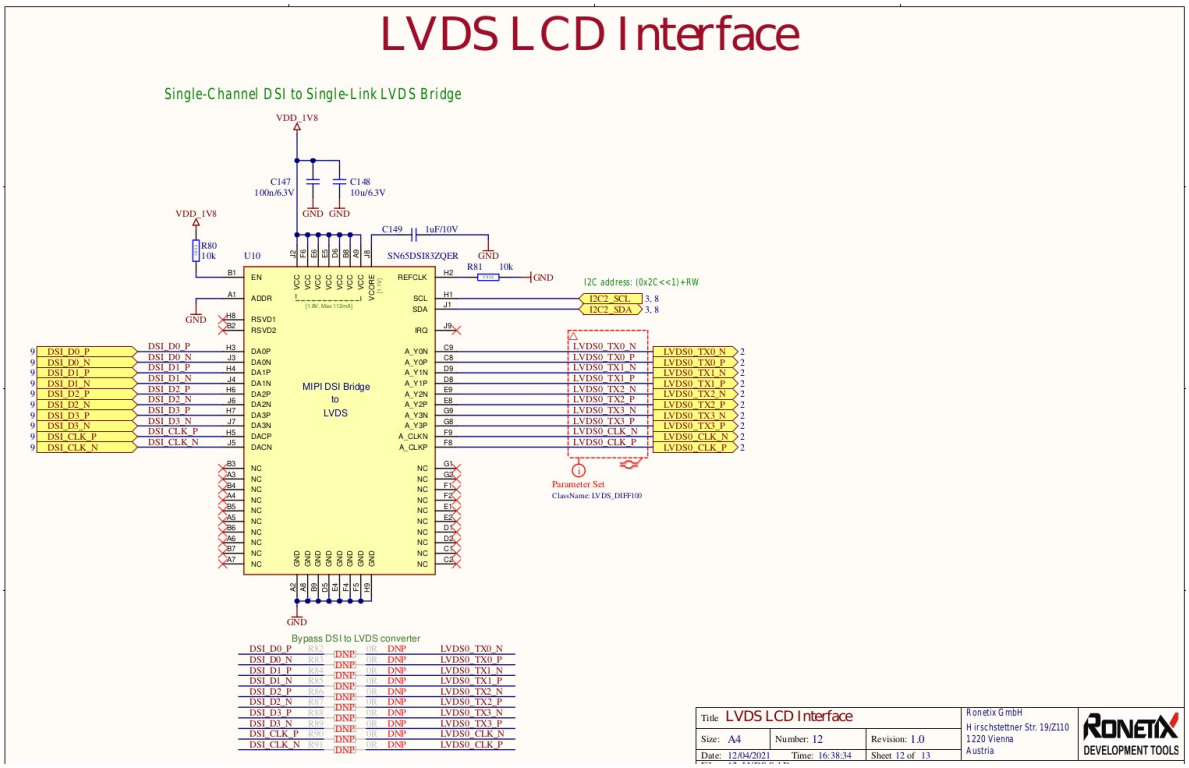


Figure 6.2: LVDS Interface

6.2 MIPI-CSI Camera interface

i.MX8M-NANO-CM MIPI-CSI interface is derived from the four-lane MIPI-CSI host controller (MIPI_CSI) integrated into the iMX8M-NANO SoC. The CSI1 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-1 specification, providing an interface between i.MX8M-NANO-CM and a MIPI CSI-1 compliant camera sensor. The following main features are supported:

- Up-to four data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Compliant with MIPI D-PHY standard specification V1.1 and Samsung D-PHY.

- Supports unidirectional Master operation
- Supports high speed mode (80Mbps - 1.5Gbps) per lane, providing 4K@30fps capability for the 4 lanes
- Support 5M pixel at 15 fps, 1080p30, 720p60, VGA at 60 fps
- Support for all CSI-2 data types:
  - RGB444, RGB555, RGB565, RGB666, RGB888
  - Legacy YUV420 8 bit
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - User Defined Data Types

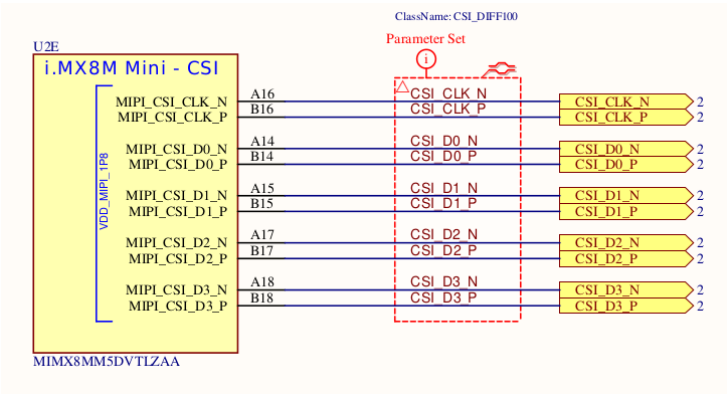


Figure 6.3: MIPI-CSI

6.3 USB interface

The i.MX8M-NANO SoC is equipped with one USB OTG controller and PHY. The USB instance contains a USB 2.0 core which supports dual-role functionality. USB2 is not available on the SoC. The USB ports support the following main features:

- High-Speed/Full-Speed/Low-Speed OTG core
- Hardware support for OTG signaling, Session Request Protocol (SRP), Host Negotiation Protocol (HNP), and Attach Detection Protocol (ADP). ADP support includes dedicated timer hardware and register interface
- up to 8 endpoints
- supports charger detection with register interface only
- Low-power mode with local and remote wake-up capability

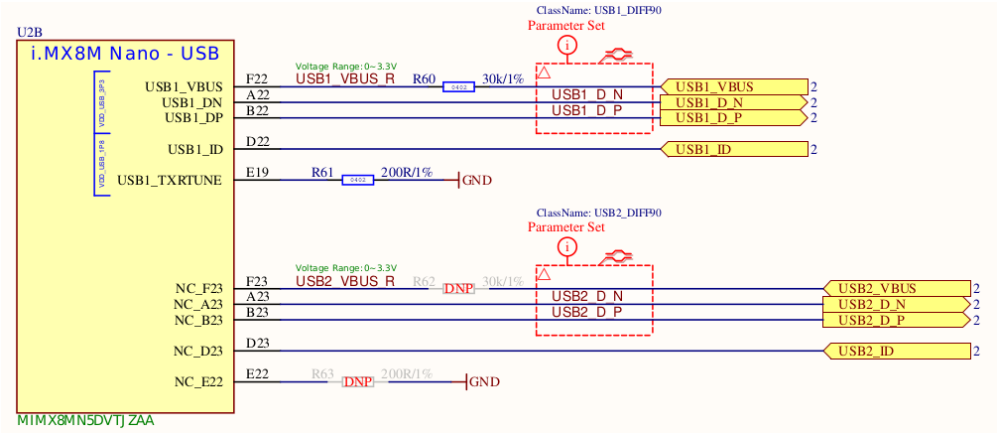


Figure 6.4: USB

6.4 MMC, SD, SDIO

The i.MX8M-NANO SoC is equipped with three MMC/SD/SDIO controller IPs (uSDHC). On i.MX8M-NANO-CM SD3 is connected to the eMMC, SD1 is connected to the WiFi module, SD2 is available on the SODIMM204 connector.

The uSDHC supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- Dedicated “card detection” and “write protection” signals
- Both 1.8V and 3.3V signaling support (uSDHC port 1 with 1-bit and 4-bit operation modes only).

6.5 UART

The i.MX8M-NANO-CM exposes up to 4 UART interfaces some of which are multiplexed with other peripherals.

The i.MX8M-NANO UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible

- 9-bit or Multidrop mode (RS-485) support
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with capability to wake the processor from STOP mode through an on-chip interrupt.

6.6 I2C

The i.MX8M-NANO SoC is equipped with four I2C bus interfaces. I2C1, I2C3 and I2C4 are available on the SODIMM204 connector. I2C2 is used internally, not available on SODIMM204. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

I2C usage table:

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1 1.8V	i.MX8-MB: Camera on CSI1	(0x3C<<1)+RW
	i.MX8-MB: USB3.0 Power Switch	(0x050<<1)+RW
	i.MX8-MB: RTC clock	(0x051<<1)+RW
	i.MX8-MB: miniPCIEe Ref. Clock	(0x6A<<1)+RW
I2C2 only on CM	1.8V, i.MX8-CM: PMIC control	(0x4B<<1)+RW
	1.8V, i.MX8-CM: LVDS	(0x2C<<1)+RW
	3.3V, i.MX8-CM: EEPROM	(0x50<<1)+RW
	3.3V, i.MX8-CM: Audio Codec	(0x1A<<1)+RW
I2C3	i.MX8-MB: PCIe M.2	
	i.MX8-MB: Camera on CSI2	(0x3C<<1)+RW

Figure 6.5: I2C address usage

6.7 SPI

Up-to three SPI interfaces are accessible through the i.MX8M-NANO-CM base board interface. The SPI interfaces are derived from i.MX8M-NANO integrated synchronous serial interface (eCSPI). Each instance of eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.

- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

6.8 Quad SPI

QSPI-A signals are available on SODIMM204 connector.

The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- DMA support.
- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

6.9 PWM

Up to four PWM output signals are available at the i.MX8M-NANO-CM base board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

6.10 Analog Audio

i.MX8M-NANO-CM analog audio functionality is implemented by the Wolfson WM8960 audio code. WM8960 is connected to i.MX8M-NANO SAI3 port.

Please refer to the WM8960 datasheet for additional details.

If the WM8960 is not populated, the SAI signals can be bypassed to the SODIMM204 connector. Either the speaker or the headphone signals can be provided to the SODIMM204 connector.

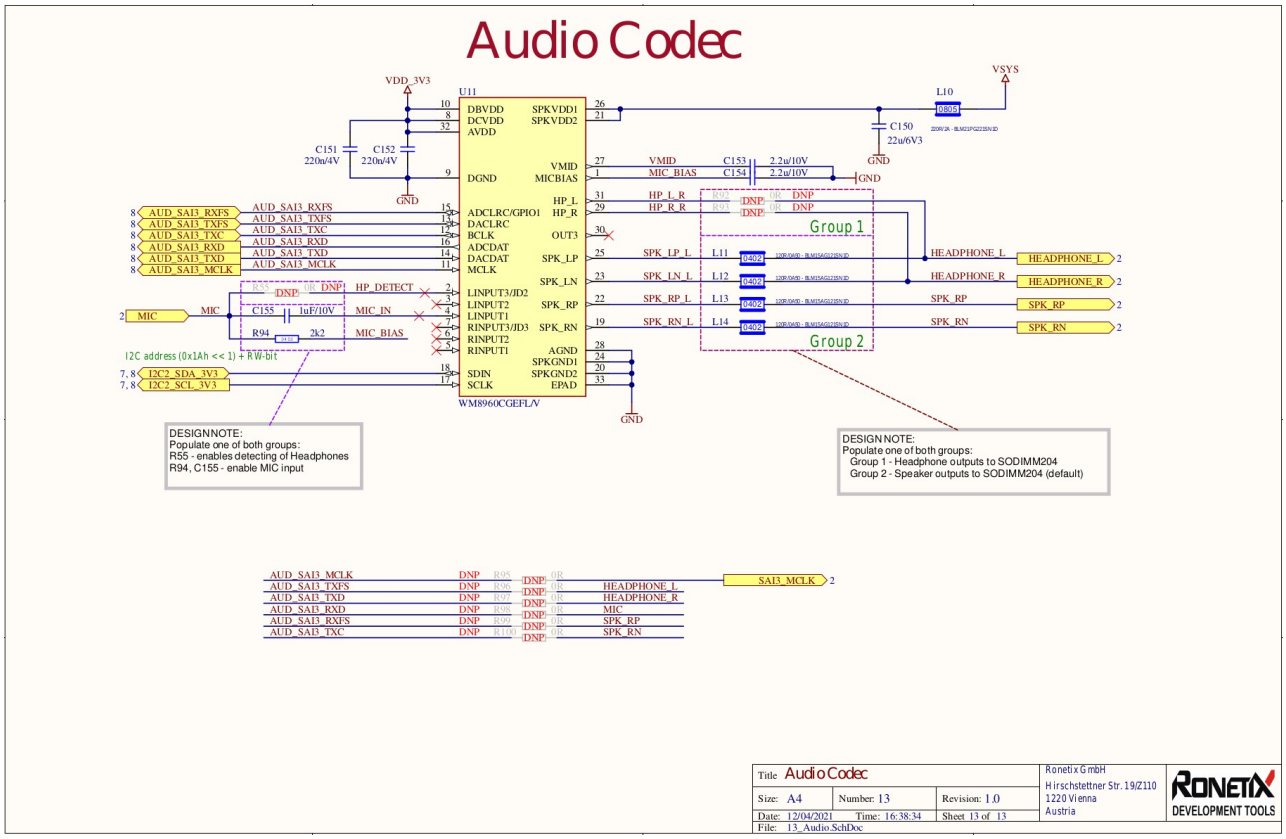


Figure 6.6: Audio Codec

6.11 GPIO

Up-to 79 of the i.MX8M-NNAO general purpose input/output (GPIO) signals are available on the SODIMM204 connector. When configured as an output, it is possible to write to an i.MX8M-NANO register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M-NANO register. In addition GPIOs peripheral can produce interrupts.

6.12 JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG signals are available on the SODIMM204.

7. Power Supply

7.1 Power supply from base board

i.MX8M-NANO-CM is powered by regulated DC supply 3.85-5.0V

Signal	Type	Description
VSYS	Power input	Main Power Supply 3.85-5.0V
GND	Power input	Common ground

7.2 Power supply provided to base board

i.MX8M-NANO-CM provides 1.8V and 3.3V power supplies to the SODIMM204 connector.

Signal	Type	Description
VDD_1V8	Power output	1.8V, Max. 0.5A

7.3 System Signals

Signal	Type	Description
MX8_ONOFF	Input with Pull-Up resistor	ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
SYS_nRST	Input	PMIC Power On signal

8. Electrical Specifications

8.1 Absolute maximum ratings

Parameter	Mln	Max	Unit
VSYS – Main Power Supply	-0.3	5.25	V

Parameter	Mln	Max	Unit
USB_VBUS - USB_HOST_VBUS, USB_OTG_VBUS	-0.3	5.25	V

8.2 Recommended Operating Conditions

Parameter	Mln	Typ	Max	Unit
VSYS – Main Power Supply	3.8	4.2	5.0	V
VSYS – recommended source capability		4.0		A

9. Operating Temperature Ranges

Range	Temp.
Commercial	0° to +70°C
Industrial	-40° to +85°C

10. Cooling

A cooling solution should be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the iMX8M-NANO-CM temperature specifications.

11. Mechanical Drawings

All dimensions are in millimeters.

The height of all parts is < 2mm.

The base board connector provides 2.8mm board to board clearance.

Board thickness is 1.0mm

11.1 Base board mounting

i.MX8M-NANO-CM SoM has two mounting holes for mounting to the base board which are plated and connected to GND.

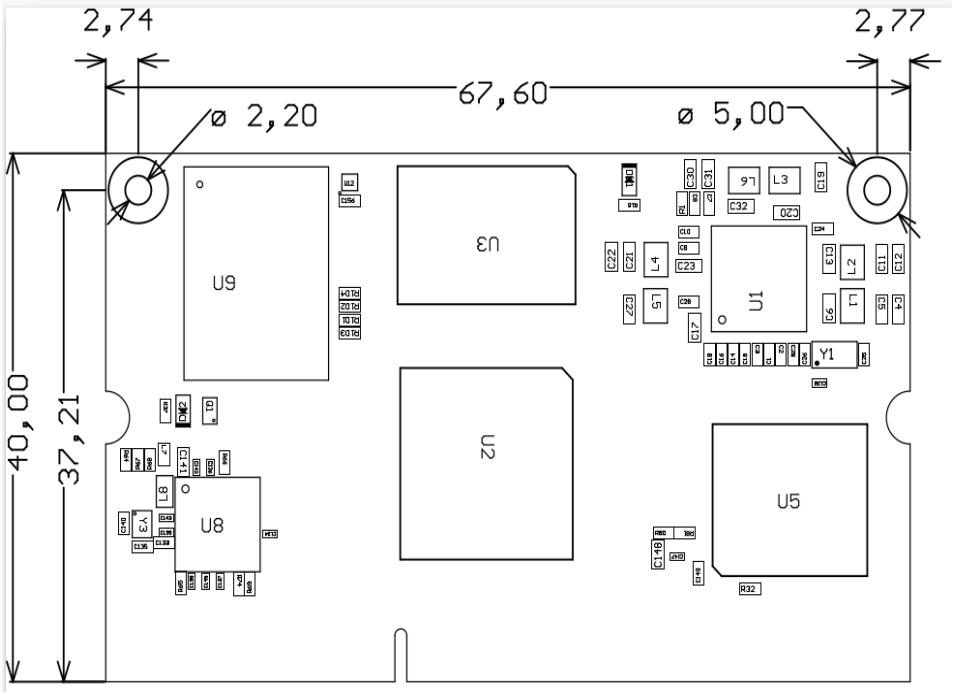


Figure 11.1: Assembly drawing

11.2 Standoffs

Fix i.MX8M-NANO-CM to the base board by mounting two spacers with suitable screws. The spacers should be:

- M2x0.4, length 3.0mm

12. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix's sole liability shall be for Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

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